

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1	"6242306"	USPAT; US-PGPUB	2002/12/30 14:51
2	BRS	L2	4	("5011787" "5021999" "5414693" "5939750").PN.	USPAT	2002/12/30 14:48
3	BRS	L3	0	6242306.URPN.	USPAT	2002/12/30 14:49
4	BRS	L4	1	(two adj bit adj non adj volatile).ti.	USPAT; US-PGPUB	2002/12/30 14:52
5	BRS	L5	7	ogura.in. and (dual adj bit).ti.	USPAT; US-PGPUB	2002/12/30 14:54
6	IS&R	L6	1154	(257/316,326).CCLS.	USPAT; US-PGPUB	2002/12/30 14:54
7	BRS	L7	107	6 and @pd>20020612	USPAT; US-PGPUB	2002/12/30 14:55
8	BRS	L12	5	("5105385" "5111270" "5330924" "5432110" "5753525").PN.	USPAT	2002/12/30 15:03
9	BRS	L15	11	("5364806" "5654917" "5864501" "5989960" "6051860" "6091633" "6133098" "6151248" "6248633" "6281545" "6329248").PN.	USPAT	2002/12/30 15:03

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 6424002 B1	37	Transistor, transistor array and non-volatile semiconductor memory	257/316	257/317	Kondo, Sadao et al.
2	US 6329248 B1	10	Method for making split gate flash memory cells with high coupling efficiency	438/267	257/E29.129; 438/304; 438/596	Yang, Yu-Hao
3	US 6281545 B1	12	Multi-level, split-gate, flash memory cell	257/315	257/314; 257/316; 257/320; 257/321; 257/322; 257/E29.308	Liang, Mong-Song et al.